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(54) METHOD AND APPARATUS FOR THE TRANSMISSION OF INFORMATION IN DIGITAL FORM

(71) We, SCHLUMBERGER LIMITED, a Corporation of the Netherlands Antilles, with administrative office at 277 Park Avenue, New York, N.Y. 10017, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a method and apparatus for transmitting information in digital form between two or more information sources and receivers. The sources and receivers may be computers and/or peripherals such as printers, card readers, magnetic tapes, magnetic drums, and so on.

Information transmission from one source to one of several receivers takes place via a common transmission system comprising a network of electrical wires or digital signal lines, currently referred to as a "bus". The invention allows information transmission between several computers, or between a computer and its peripherals, or even between several computers and peripherals associated with other computers.

Hereinafter, all devices capable of generating information to be transmitted will be regarded as sources while all devices capable of using received information will be regarded as receivers. Of course it will be recognized that some devices are capable of both transmitting and receiving functions and will be regarded as a source when transmitting and receiver when receiving.

There are different known methods for performing a transmission between several information sources and receivers. In the case of a transmission between a computer and its peripherals, use is made of a bus connecting the different sources and receivers of information to each other. Information transfer from a source peripheral to a receiver peripheral device generally takes place under the control of the computer. To achieve this, for example, the information to be transmitted is first transferred from the source peripheral to registers or memory of the computer and then transferred from the computer to the recipient peripherals. These transfer operations are carried out following instructions given by the computer and are synchronized by the computer's own time base. When two computers are conversing with each other, they are generally connected by a bus and the information is transferred from the memory of one to the memory of the other.

An initial difficulty arises when the sources and receivers are made by different manufacturers. In this case, it is not possible to connect them to each other because their outputs and inputs are not compatible, i.e. the messages transmitted by the source are not intelligible to or assimilable by the receiver, from the standpoint of electrical characteristics as well as from that of the code or the format of the information. In this case, at each output and input of the bus, use is made of an interface whose role is to ensure the compatibility, i.e. the intelligibility, of the messages sent by the source in question to the others.

Another difficulty stems from time lost by the computer controlling the information transfers.

Frequently, because the synchronization between computer memories required during transfers prohibits any other possibility conflicting use which could change its timing, the controlling computer must essentially be dedicated to this operation during the transfer time. Even sophisticated computers usually require the transfer time to be "stolen" from some part of its cycle time.

The U.S. patent No. 3,810,103 provides a solution to this problem. The main teaching of that patent is that the transfer of data from a transmitting source to different receivers can be achieved asynchronously with respect to the time base of the computer by relegating the transfer-rate timing to the receiver. Each receiver has means for indicating that it has received a transmission, and means for indicating to the computer when it is ready to receive another transmission. It may however be noted that the transfer

transferring the information thus received to the source or sources to which the receiving memory or memories is or are assigned, under the control of the receiving source;

wherein an order of priority is determined for the transfer of said information via said bus with the application of a strategy.

The invention will now be described, by way of example only, with reference to the accompanying drawings, of which:

FIG. 1 illustrates a method of information transmission and shows schematically transmission apparatus including only one bus;

FIG. 2 shows apparatus which may be employed to transmit between two buses;

FIG. 3 shows schematically a possible transmission system in which three buses are used;

FIG. 4 represents schematically the structure of an information file as it is stored in a multiword memory associated with an information source;

FIG. 5 illustrates how selected receivers are indicated in a file to be transmitted;

FIG. 6 illustrates schematically the process used for transmitting the information;

FIG. 7 shows schematically the connections of an interface with the bus;

FIG. 8 is a block diagram of an interface connected, on the one hand, to an information source and receiver and, on the other hand, to the bus;

FIG. 9 represents a simplified interface allowing the transmission of an information file containing only one word;

FIG. 10 represents in detail an embodiment of the memory part of an interface;

FIG. 11A, 11B, 11C, 11D, 11E, and 11F represent in detail an embodiment of the logic circuits of an interface;

FIG. 12 illustrates the different instructions sent by the supervisor;

FIG. 13 represents the block diagram of a supervisor;

FIG. 14 represents in detail a part of an embodiment of the supervisor;

FIG. 15 represents an embodiment of the file length counter of the supervisor;

FIG. 16 illustrates a method, or strategy, allowing the supervisor to assign an order of priority to each source among several requesting sources wishing to transmit at the same time;

FIG. 17 represents a particular embodiment for implementing the strategy; and

FIG. 18 illustrates the timing of various logic signals generated and utilized by the circuits shown in the above Figures.

Computers are normally equipped with a certain number of input and output terminals which allow them to be connected with peripherals or with other computers. Messages or information to be transferred are organized in the form of information files. These files are made up of one or more words each comprising the same number of bits. This number of bits is in general sixteen, sometimes eight if the computer is small and sometimes thirty-two or more in the case of a more powerful computer. In the following description, the illustrative embodiment of the invention uses information files consisting of identical words each having sixteen bits. This figure is of course given only as an example.

In one regard, an information source may be considered as a "talker" and the receivers of the information considered as "listeners". In this regard, computer buses provide, in addition to the 16 basic data lines, a bus wire or signal line for designating which of these functions are to be performed. Logic signal levels such as "0" or "1" are sent on this line for this purpose and will be referred to hereinafter as TFLG or LFLG (standing for "talker flag" and "listener flag"). Devices interfaced to the bus also use the logic levels "0" or "1" to indicate that a "talker" has information to transmit or a "listener" is ready to receive. Other lines commonly provided on such buses are a data read or write wire, and finally, at least two additional wires left available to the user.

The method and apparatus for transmitting information between different sources and receivers described herein uses only these output and input wires or lines, whatever the type of computer or peripheral. The terms wire and line will be used interchangeably herein, contemplating use of either electronic or photo-optic connections such as light pipes, for example, in the latter case.

It is evident that the present system would offer limited advantage in connecting two computers of the same type and manufacturer because, in that case, it is sufficient to directly connect the different input and output terminals to each other by means of a suitable coupling. On the other hand, the present invention would provide the advantage of relieving both computers of the bus supervision constraint. When a larger number of computers and/or peripherals have to be connected to each other, a highly-complex direct connection is involved, and the present invention makes it possible to achieve the connection of the different sources and receivers to each other without restriction.

In FIG. 1 is show how the different transmitting and/or receiving sources are connected in accordance with the present invention. With each information source and/or receiving device 2 is associated an interface 4 which is connected to a bus 6. A source 2 can be of the type that only transmits information and, in this case, it is represented by Si and an arrow running from its associated interface 4 to network 6. A

transmit information to devices 28 of bus 32 via intermediate stage 38A and, conversely, from devices 28 of bus 32 to devices 22 on bus 12 via intermediate stage 38B. Information transmission is also possible from devices on bus 6 to devices of bus 32 through the intermediate stage 42. Devices transmitting most frequently with each other are preferably grouped on the same bus such that transmission throiugh an intermediate stage from one bus to another occurs less frequently than single bus transmissions.

To transmit information from bus 6 to bus 32, as shown in FIG. 3, intermediate stage 42 may be used. It is also possible to transmit first from bus 6 to bus 12 through intermediate stage 14A and then from bus 12 to bus 32 via intermediate stage 38A. If the transmissions between bus 6 and bus 32 are rare, intermediate stage 42 may be superflous.

It is noted that transmission of information takes place asynchronously from two viewpoints. First of all, if we consider a system having only one bus, as shown in FIG. 1, the time base of the bus transmission system is that of the supervisor and not that of the device(s) connected to the bus line, even if one device is a computer. This is easily understood because the information files transit in the memories of the interfaces and, once in the memories, the assembly formed by the interfaces and their associated memories, the supervisor and the bus may be regarded as independent of the information source and/or receiving devices. Also, if a system equipped with several buses is considered, the time bases of the different bus supervisors are independent of each other.

If we consider the transmission of information from a source device to its associated memory in its interface, the time base is that of the source rather than that of the bus supervisor. If we consider the transmission of information from the memory associated with a receiver device in its interface, the time base is that of the receiver, which is independent of the time base of the information source or that of the bus supervisor. The only time relationship is that transmission from the source to source-associated memory must precede that from source-associated memory along the bus to receiver-associated memory to the receiver.

It has already been indicated that the information to be transmitted is organized in the form of a file. Each file is composed of a specified number of words, varying from one to several words. Each word is composed of a given number of bits. FIG. 4 represents, as an example, the structure of an information file which can be stored in the memories of the interfaces and is the particular case where the transmitting bus has sixteen input wires and sixteen output wires. Each word, represented by number increasing along the direction of arrow A, has sixteen bits noted from 0 to 15 in FIG. 4, represented by numbers increasing along the direction of arrow B. The information file can include up to 256 words, noted from 0 to 255 in FIG. 4. The structure of 256 words of sixteen bits each of course represents only an example and is not limitative. The figures 0 to 255 indicated by the arrow A also represent the addresses in memory at which the information file is stored.

For example, address 0 is the first word, and can be used to specify the length of the file; i.e., the number of words to be transmitted. Thus, each file is not fixed at 256 words. The file can contain information relative to the receiver(s), for example, the addresses of the information to be transmitted. For example, the word at address 1 can be reserved to indicate the addresses of the information to be transmitted when one bus is used. The word written at address 2 can contain the addresses for devices on bus 2; the word at address 3, the address for the devices on bus 3, and so on. The rest of the available words of the information file are reserved for the information proper. It is evident that all the words in a given file need not contain information. It may then be advantageous to transmit only the words containing the information, as indicated by the file length information contained in word 0, for example. The indication of the source of the information; i.e., of the source device address, can be entered in the information file but this is not a necessity. The information contained in the file may concern commands from one source to one or several receivers and/or data proper. Command words and data words are transmitted on the same wires of the bus. The supervisor ignores the words in the files except for those assigned to file length, addresses, etc.

FIG. 5 shows a very simple way to indicate each device selected to receive the information file. The indication is made by means of the bits of an assigned word. It is assumed that there are no more than sixteen devices connected to a given bus. The word address 1 corresponds to bus number 1, address 2 to bus number 2, and so on. To each bit 0 to 15 of address word n is assigned a device on bus n. If the bit corresponding to a given device is in a given logic state, 0 or 1, this will mean by convention that this device is the addressee of the information file. Thus, in the example of FIG. 5, where a "1" state indicates the receiver, devices 0, 3, 4, 5, 7, 9, 10 and 13 are the selected addressees on bus number 1, and devices 0, 1, 3, 5, 6, 11, 13 and 14 are the selected addressees on bus number 2.

interface to indicate that its listening or receiving memory is not available; e.g., its contents have not been transmitted to the receiving device and is thus write protected.

The wire located in FIG. 7 to the right of the data wires 0 to 15 and whose transmitter and receiver are hachured is an additional wire used for assigning a number to each of the interfaces and associated devices and hence for individualizing them. To achieve this, this "hachured" wire is connected to the particular one of data wires 0 to 15 equal to the number of the interface and device (in FIG. 7, for example, this hachured wire has been connected to the data wire 13 which means that the illustrated interface has been assigned the number 13). This method of individualizing the interfaces has two advantages: firstly, all the interfaces can be constructed in the same manner (it is only during the set-up of the transmission system that they are individualized) and, secondly, the interfaces are not assigned an address in the usual sense of the word. It may be noted that if two transmitting interfaces connected to the same bus bear the same number, there has been a wiring error.

Summarizing, the illustrated interface has twenty-two electrical connections, sixteen information wires used both for the inputs and outputs of the interfaces and six wires used for the "supervision" of the bus system: three wires for receiving instructions from the bus supervisor, a PLS signal wire to indicate that an instruction is being sent by the supervisor, wire B to indicate the availability or non-availability of the device-associated memory within the interface to be written into or, alternatively, write-protected, and finally, a "hachured" wire allowing a number to be assigned to each interface.

FIG. 8 represents schematically an interface connected, on the one hand, to a source and/or a peripheral receiving device 66 and, on the other hand, to bus 6. The interface has two distinct parts: a "listener" portion which makes it possible to receive by means of the receivers R data coming from the bus and a "talker" portion making it possible to transmit information on bus 6 by means of transmitters E. In FIG. 8, transmitters E and receivers R are each shown schematically by a single triangle. A more detailed, but quite schematic representation has been given in FIG. 7. Each "listener" or "talker" portion has identical device-associated memories, namely a listener memory 70 associated with an information receiver or a talker memory 72 associated with an information source, word counters 74 or 76 connected to the respective memories and a flip-flop 78 or 80 having one output Q and two inputs S (set) and R (reset). These different elements are connected to the bus 6 by means of a logic circuit 82.

In general, every computer bus has inputs and outputs enabling the transmission of information to and from a peripheral device. To transmit information, peripheral devices usually have at least output data wires 84, with as many output wires as there are bits in its information word (sixteen in the described example), an optional signal FTD (file transmitted) left at the disposal of the user, a signal wire TFLG (talker flag) to indicate that it has sent information, and finally, a wire WTD (word transmitted) on which is sent a signal whenever the device sends a word. For the reception of information, the device has inputs 86, the number of which is equal to the number of bits there are in its information word (sixteen in our example), a signal FAD (file accepted) left at the disposal of the user, a signal wire LFLG (listener flag) to indicate that it has received the information and, finally, a wire WAD (word accepted) on which is sent a signal whenever the device reads an information word.

Assuming that peripheral device 66 requests transmitting a file to one or several receivers through the bus 6; then device 66, acting as a source, first examines the logic state of the input TFLG: if TFLG is in logic state 1 this means, for example, that the talker memory 72 is empty. If TFLG is in logic state 0 this means, on the contrary, that the talker memory 72 is still protected from being written into. Assuming that the talker memory 72 is not write-protected and is available (TFLG=1), it will be automatically preset at the address 0. Device 66 then transmits an information word on its outputs 84 to talker memory 72. A signal is also sent by device 66 at this time on its output WTD to logic circuit 82, indicating "word transmitted". This signal allows the writing of the word transmitted by the device into talker memory 72. Moreover, for each WTD signal received by logic circuit 82, a signal TINC (talker increment) is transmitted by circuit 82 which increments memory-word counter 76 by one row. Thus, since the talker memory 72 was initially preset at address 0, and the WTD signal results in a TINC signal which increments counter 76, counter 76 then indicates address 1. When device source 66 has finished sending its information file, it supplies a signal FTD which is applied to the input R of flip-flop 80, thereby placing the output Q; i.e., the signal line TFLG, in logic state 0.

The output Q of the flip-flop 80 is placed in the logic state 0 by the source 66 when it has finished writing in the talker memory 72, as described above, and placed in the logic state 1 by a signal transmitted by the

ory stages 90, 92, 94 and 96. Counter 74 of the "listener" part is represented by the two counter stages 98 and 100. The large horizontal rectangle 102 represents schematically the connection of listener memory 70 to the receiving portion of a device by means of the sixteen information input terminals 104 in the device. The sixteen inputs 106 in memory 70 in the form of 4 bit counters are connected to receivers in circuits 134 indicated by R. Counter 74 in the form of 4 bit counter stages 98—100 has eight output wires 108 representing the eight address wires of memory 70. Wire LMR is used for resetting counter stages 98—100 as previously discussed in regard to counter 74. Whenever counter 74 is to be incremented by one row, a signal LINC is sent on the corresponding wire to the counter. Input LR/W is used to preposition talker memory 70 in the reading or writing position. When the bus transmits information to be entered in the memory, the memory is prepositioned in the writing position. When the receiving device reads from the memory the reading position is chosen. The large horizontal rectangle 110 represents connections between the interface and the bus. To each of the 16 data line connections 112 between the interface and the bus are connected a transmitter E and a receiver R. The receivers R are connected permanently to the bus.

The four rectangles 114, 116, 118 and 120 of Fig. 10 represent talker memory 72 of FIG. 8. The two 4-bit counter stages 122 and 124 represent counter 76 of FIG. 8. Counter stages 122—124 have eight output wires connected to eight address wires 126 of memory 72. This memory is connected to sixteen information outputs in the source portion of the device by means of the connector 128 and sixteen terminals 130. Sixteen outputs 132 of memory stages 114—116—118—120 of memory 72 are connected to transmitters E in circuits 134. Input TMR to counter stages 122—124 of counter 76 makes it possible to reset counter 76 and thereby choose the address 0. Input TPL to counter stages 122—124 allows prepositioning of counter 74 at a given address. This input TPL is particularly advantageous when the transmitting and receiving system has several buses. Receivers indicated by information stored at memory addresses corresponding to the bus through which the file stored in the memory is to be transmitted, can be selected by means of the signal TPL. Input TR/W to memory 72 makes it possible to preposition memory 72 in the reading or writing position.

The four circuits 134 shown connected to bus 6 in FIG. 10 act as switches I (FIG. 7) allowing the connection of transmitters E to bus 6. When input 136 of circuits 134 are in logic state 1, transmitters E are disconnected from the bus and are connected when their logic state is 0. The connection of transmitters E to the bus depends also on the logic state of the outputs of OR gate 140 and AND gate 138. For transmitters E to be connected to the bus, it is necessary that four instructions FIT, GRL, GPL and OLF all be present in addition to a signal designated as TALK. The meaning of these first four signals, which correspond to instructions sent by the supervisor, was briefly described in regard to FIG. 6 and will be described further with reference to FIG. 12.

By way of example, transmitters E can be made up of open-collector NAND gates and receivers R can be simple inverters or adapters. Circuits 134 can be integrated circuits of the MC 3443 type; memory stages 90, 92, 94, 96, 114, 116, 118 and 120 can be integrated circuits of the 5101—2 type, and counter stages 98, 100, 122 and 124 can be integrated circuits of the 74 LS 197 type.

FIGS. 11A, 11B, 11C, 11D and 11E represent in detail embodiments of logic circuits 82 of an interface. These logic circuits allow generation of the previously described signals LINC, TINC, LR/W, TR/W, TPL, LMR and TMR indicated in FIGS. 8, 9 and 10.

FIG. 11A represents decoding circuit 150 equipped with three inputs 152 to which are applied the instructions coming from the supervisor. Referring to FIG. 7, it was indicated that the instructions from the supervisor are conveyed through wires 16, 17 and 18. From logic instruction signals applied to inputs 152, circuit 150 provides signals corresponding to instructions TAC, GRL, OLF, GFL and FIT in negative logic, as indicated by lines or bars over these designations, as for example, $\overline{\text{GRL}}$. The latter four instructions were discussed in regard to inputs to AND gate 138 shown in FIG. 10. Where positive logic or the inverse of one of these signals is required, an inverter may be employed, as is well known by those skilled in digital logic circuitry.

FIG. 11B represents a part of logic circuit 82 allowing the generation of signal LMR used generally as listener memory reset but also for resetting a memory-word counter (counter 74 or its stages 98—100 respectively in FIG. 8 or 10) associated with the listener memory of an interface. The "listener"-memory reset LMR signal is generated when certain events occur, as achieved by means of NOR gate 154 and AND gate 156, as for example, when the transmission system is reset to its initial state (this is accomplished by instruction INI sent by supervisor as discussed in regard to FIG. 6 at block 43),

memory. Signal LSTN thus controls the output of the NAND gate 176, protecting the contents of memory 70 when appropriate.

However, it is still necessary for counter 74 associated with listener memory 70 to be incremented by signal LINC (shown in FIGS. 8 and 10) whenever an information word has been transmitted from memory 70 to the receiving device. It will be recalled from the description of FIGS. 8 and 9, that for each word transmitted, signal WAD is sent by the receiving device. In this case, it is NAND gate 182, shown in FIG. 11E, receiving on its two inputs signal LSTN and $\overline{\text{WAD}}$ (in negative logic, $\overline{\text{LSTN}}$ and $\overline{\text{WAD}}$, respectively) which causes the appearance of the 500-nanosecond signal at output Q of flip-flop 172. Thus, the sending of signals WAD by the receiving device, in the absence of enabling signal LSTN, now causes the appearance of signal LINC, and not the supervisor's FIT signals as in the case where signal LSTN enabled writing into memory 70.

FIG. 11F represents an embodiment of a part of logic circuit 82 making it possible to write or read information in "talker" memory 72 (FIGS. 8 and 9) or stages 114—120 (FIG. 10). As shown in FIG. 11F, C—D flip-flop 184 is connected: to receive on its C input, NAND gate 186 output which receives logic signal $\overline{\text{TALK}}$ and $\overline{\text{WTD}}$; to receive on its S input NAND gate 188 output, which receives on its two input signals TALK and FIT; to output at Q to NAND gate 190 and transmitter 195; and to output at $\overline{\text{Q}}$ to a 500-nanosecond delay line 192. Transmitter 195 output is connected to a 200-nanosecond delay line 196 which inputs to differentiator circuit 198 (like that already described) to deliver signal TINC. NAND gate 190, which delivers signal TR/W on its output, receives on its two inputs the signal $\overline{\text{TALK}}$ and the 500-nanosecond signal transmitted from output Q of the flip-flop 184. Differentiator circuit 198 transmits signal TINC at its output 200-nanoseconds after TR/W as with LINC and LR/W for the similar circuits shown in FIG. 11E.

Assuming that TALK=1, which means that "talker" memory 72 has information to transmit on the bus, it is necessary to protect memory 72 from being written into and changed. To achieve this, signal TR/W is left in logic state 1, protected by the $\overline{\text{TALK}}$=0 input to gate 190. To transfer a word from the "talker" memory 72 to bus 6, the supervisor sends instruction FIT, which in the presence of the TALK=1 signal at gate 188 results in output Q. In this case, signal TR/W is left in logic state 1 because logic state $\overline{\text{TALK}}$=1 necessary to cause TR/W is not present as input to NOR gate 190. However, logic signal TINC is delivered by logic circuit 82 each time a word is transmitted to bus 6 so as to increment counter 76 associated with "talker" memory 72.

On the other hand, when the logic state for signal TALK indicates that the source device can transmit information to "talker" memory 72, memory 72 is then placed in the enable writing position by the change-over of signal TR/W to the appropriate logic state. This occurs when signal $\overline{\text{WTD}}$ is applied to one of the two inputs of the NAND gate 186. Signal WTD is sent by the source device whenever it has transferred a word to be written into the "talker" memory as described in regard to FIG. 8. After the appearance of signal TR/W, signal TINC is delivered after a 200-nanosecond delay caused by delay line 196. Signal TINC thus increments memory-word counter 76 associated with talker memory 72 but now during a write process.

The logic of the bus supervisor will now be described. The supervisor sends instructions to the different interfaces so as to control the transfer of files between interfaces. These instructions are represented schematically in FIG. 12. Referring to FIG. 7, it was mentioned that bus 6 has, notably, three wires 16, 17 and 18 to carry the instructions transmitted by the supervisor. These wires are represented schematically again by 16, 17 and 18 in FIG. 12.

To control the transfer of files between the different interfaces, the supervisor sends instructions to these interfaces. Eight such instructions are described in this illustrative embodiment, the list of which is given in FIG. 12. These instructions are conveyed by bus 6 on the electrical wires 16, 17 and 18. Instruction INI (initialization) corresponds to logic states 0, 0, 0 on electrical wires 16, 17 and 18 respectively and causes the general resetting of the system. This is accomplished when, for example, the communication system is started up or by actuation of a reset control. In response, all transmitters E (see FIG. 7) of the different interfaces are disconnected from the bus by the opening of switches I in the interfaces as already described.

Instruction TAC (talker acknowledgement) is transmitted to allow the supervisor to determine whether one of the interfaces has information to transmit. This instruction also opens, again, switches I of trans-

R of the interface shown in FIG. 7. As with the interfaces, receivers R can be adapters and transmitters E can be open-collector NAND gates. Transmitters E at block 202 of FIG. 13 are connected to the information wires 0—15 of the bus and are associated with switches I as in the case of FIG. 7, represented schematically in FIG. 13 by arrow 204. By contrast, transmitters E at block 206 of FIG. 13 are connected to instruction wires 16, 17 and 18 of bus 6. Initially, logic circuit 208 of the supervisor sends instruction INI on bus 6 by means of transmitters E shown at block 206. Logic 208 then increments instruction counter 210. This instruction counter is associated with instruction memory 214 in which have been written the instructions shown in FIG. 12. Thus, whenever an increment signal is input at 212 to counter 210 by logic 208, a new instruction address in memory 214 is generated and its instruction sent on wires 16, 17 and 18 of the bus. An example of the possible content of memory 214, showing instructions in code form is given in FIG. 12.

It will be recalled that the selected source file length is present on the bus during the GFL instruction. At this time, the file length is recorded in counter 216 shown in FIG. 13 by a signal applied to its input 218. When several interfaces have a message to be transmitted at the same moment, logic circuit 208 calls on strategy circuit 220 which determines a priority as already discussed and as will be described in regard to FIG. 17. The timing for sending the different instructions, as well as for the transmission on the bus, is performed by clock H connected to bus 6.

Initially, instruction INI is sent on instruction wires 16—18 by transmitters E at 206 to the different interfaces. Then, instruction counter 210 is incremented and instruction TAC appears at the output of the memory 214 and is sent on transmitters E at 206. If none of the interfaces wishes to transmit information, instruction counter 210 is not incremented and the supervisor will thus continue to send the instruction TAC. When an interface has information and makes a request to transmit, instruction counter 210 is incremented and the instruction sequence continues to instruction OTF which is sent on the bus from memory 214. In the same manner, instruction GRL is sent when instruction counter 210 is again incremented. Now, if instruction GRL shows that the requested transmission is not possible because one of the addresses for the transmission is not available, instruction counter repositions the memory at its address corresponding to previous instruction TAC (see FIG. 6 at blocks 52, 54 and 56). On the other hand, when the transmission is possible, the address of memory 214 will be incremented and instruction OLF sent so as to "open" the addresses of the requested transmission. Next, instruction GFL is sent so as to get the length of the file to be transmitted from the source (stored in word 1 of its associated memory). This length is then read into counter 216 of the supervisor. Word-by-word transmission is then performed by repeating instruction(s) FIT, each docrementing counter 216 via input 218, until counter 216 reaches zero. A "done" signal is then sent from counter 216 to input 222 of logic 208.

FIG. 14 represents in detail a particular embodiment of logic circuit 208, instruction counter 210, and memory 214 of supervisor 8. In FIG. 14, circuit 224 shows the equivalent of the memory 214 as well as part of logic circuit 208, the rest of logic circuit 208 being represented by decoding circuit 226 shown in FIG. 14. Instruction counter 210 is represented in detail. Circuit 224 shown in FIG. 14 is made up of an assembly of AND gates 230, NAND gates 232, OR gates 234 and inverters 236. The different instructions applied to the input of these logic gates are represented in FIG. 14 using the terminology of FIG. 12. Signal BR indicates that all the interfaces requesting to transmit information at a given moment have in fact transmitted their information (this will be explained in the description given with reference to FIG. 17). Signal DONE is applied to the input 222 of the logic circuit 208 (FIG. 13) by counter 216 when its count has been decremented to zero at the end of the transmission of a file. The logic used can be negative: this is the reason for the presence of lines over certain instructions to indicate that it is the inverse of the logic signal shown which is considered. The inverse of a logic signal is obtained easily by means of an inverter such as inverter 236.

Instruction counter 210 includes essentially three identical flip-flops 238 which can be, for example, integrated circuits of the 74 LS 74 type. On inputs 240 of flip-flops 238 are applied clock signals H. On second inputs 242 of flip-flops 238 are applied signals coming from circuit 224, as represented in FIG. 14. Output of each flip-flop 238 represents one of three transmitters E at 206 (FIG. 13) of the memory 214 which are connected to the three instruction wires 16—18 of bus 6. Outputs 244 of flip-flops 238 in instruction counter 210 are thus used to generate the instructions as represented schematically in FIG. 12. Outputs 244 of instruction counter 210 are also applied to three inputs of decoding circuit 226 which furnishes at its eight outputs 246 instruction signals, both positive and negative, for the eight instructions shown in FIG. 12. Circuit 226 can be, for example, an integrated cir-

and all requests from the first illustrated review have been granted.

At moment 4, a new review is made by sending instruction TAC and storing the responses (TACM). The stored result shows that device 1 requests to transmit to receiver 4 and device 3 requests to transmit to receivers 2 and 1. The available addressees are 1, 2 and 4. The result is that device selected as source is device 1. At the following moment, there remains the request of device 3 requesting to transmit to receivers 2 and 1. Available addressees are 1 and 2 since device 1 is in the process of transmitting to receiver 4. Device 3 is selected as the last source.

At moment 6, instruction TAC is transmitted for a new review and its result is stored. Devices 1 and 2 request to transmit respectively with receivers 2 and 3 and 1 and 3. The available addresses are 3 and 4 since the source or talker part of device 3 is in the process of transmitting to receivers 2 and 1 which are thus no longer available. Thus, the request of the device 1 can not be satisfied since receiver portion of device 2 is no longer available. Likewise, the request of device 2 cannot be satisfied, since receiver 1 is not available (still receiving from 3), although address 3 (the receiver portion of device 3) is available. This results in a "PAUSE" in the strategy for the moment. Then, following at moment 7, the same requests are found as at moment 6 but the available addresses are changed, in this case; 1, 2, 3 and 4 are now available. The result is that the device selected as the next source is device 1. At moment 8, there remains the request of device 2 requesting to transmit to addresses 1 and 3. Available addresses are 1 and 4. The address 3 is no longer available because device 1 is in the process of transmitting to it. There is thus another PAUSE. Finally, at moment 9, the request of device 2 is satisfied.

FIG. 17 shows, as an example, an embodiment of the above-described strategy (220 in FIG. 13). Strategy circuit 220 of supervisor 8 includes sixteen J—K flip-flops 280; i.e., as many flip-flops as there are data wires in bus 6. Each data wire is associated with one flip-flop and is connected to input 282 of AND gate 284 having a second input 286. Outputs of AND gates 284 are connected to the J input of flip-flops 280. The $\overline{Q}$ output is connected to input 288 of the two inputs of NOR gate 290. The second input 292 of NOR gates 290 receives in a cyclic manner an authorization signal from logic circuit 208, as shown in FIG. 13. In other words, inputs 292 each receive separate authorization signals, one after the other. Outputs 294 of NOR gates 290 are connected to the transmitters E (202 as shown in FIG. 13) of supervisor 8. Outputs 294 of NOR gates 290 are also connected, on the one hand, to the K inputs of flip-flops 280 and, on the other hand, to the inputs of NAND gate 296 via inverters 298.

Each R input of flip-flops 280 is connected to switch 300 making it possible to connect the R input either to ground or to the output of NAND gate 302 which receives on its two inputs instruction INI and the bus signal PLS. Switches 300 indicate whether or not requests from the corresponding interfaces should be considered. If the R input of a flip-flop 280 is connected to ground, output $\overline{Q}$ is held in logic state 1 and, in this case, if an authorization signal should be present on input 292 of gate 290, the logic state of the output from gate 294 will remain at 0. Considering that a logic state 1 on this output means that the corresponding interface is selected, grounding of R input by switch 300 corresponds to disconnecting the interface corresponding to this flip-flop and data wire.

Each output $\overline{Q}$ of the flip-flops 280 is connected to one of the inputs of NAND gate 304 whose output is connected, via inverter 306, to one of the two inputs of AND gate 308. The second input of this gate receives instruction TAC. The output of gate 308 is connected in parallel to inputs 286 of AND gates 284.

The operation of strategy circuit 220 is the following: the initial state of output $\overline{Q}$ of flip-flop 280 is logic state 1 (permanent state if switch 300 grounds R input). When all $\overline{Q}$ outputs are in logic state 1 (this corresponds to no requesting devices), NAND gate 304 outputs logic state 0, which is inverted to logic state 1 by inverter 306 and applied to one of two inputs of AND gate 308. Instruction TAC then can enable AND gate 308 to output logic state 1 which enables one input to AND gates 284. If a request remains (the yet unauthorized device will have its flip-flop output $\overline{Q}$ still in logic state 0), at least one output $\overline{Q}$ will not be in logic state 1, causing NAND gate 304 output to be in logic state 1 and in turn AND gate input 286 to be in logic state 0. This thereby disables input J to all flip-flops 280 and prevents storage of further requests until all $\overline{Q}$ outputs are returned to state 1. At this time, instruction TAC brings all inputs 286 to enabling state 1 and flip-flops 280 can again store the logic state present on their individual inputs 282. Thus, this TAC instruction has the meaning

information source device to at least one receiver device selected from several devices interfaced to a common transmission bus. Each device transmits asynchronously at its own rate, independent of the transmission rate of the bus. Each device having information to transmit first transmits at its own rate to its interface, and in particular to an associated memory within its interface. When this transmission is complete, the device requests the transmission of the contents of this memory to specified receiving devices. A bus supervisor periodically polls the devices for such requests and determines which requesting device will act as an information source. Transmission is then initiated from the source-device associated memory along the bus at bus rates to memory(ies) associated with the specified receiver device(s). When this transmission is complete, transmission occurs from the receiver-associated memory(ies) to the receiving device(s) at rates and times particular to each receiving device. In this manner, maximum advantage is made of the transmission capability of the bus system.

WHAT WE CLAIM IS:—

1. A digital information exchange system comprising a multiplicity of information sources and information transmitting means, said information sources including at least two emitting sources and at least one receiving source, and said information transmitting means interconnecting said information sources and including: a bus having transmission wires for transmitting both data and source control words; a multiplicity of interfaces, each of which connects an associated one of said information sources to said bus and is provided with a memory in which information to be transmitted from the associated source to said bus, or vice versa, can be temporarily stored, said information being stored in the memory in the form of an information file comprising at least one control or data word; and a supervisor connected to said bus for controlling the information transfer via said bus, said information being transmitted along said bus asynchronously with respect to said sources, wherein said supervisor comprises means for storing system operating instructions, each interface comprises means responsive to said system operating instructions, and said bus comprises instruction wires for transmitting instructions between said instruction storing means and said instruction responsive means, one of said instructions allowing said supervisor to check the interface of each emitting source simultaneously to determine whether it has a data file to transmit.

2. The system of claim 1, wherein at least one of said information sources is a computer.

3. The system of claim 1 or claim 2, wherein said information file includes several words each made up of the same number of bits.

4. The system of claim 3, wherein each information file includes the address of the source or the addresses of the sources to which said information file is to be sent.

5. The system of claim 4, wherein said addresses are contained in the same word, each of said sources corresponding to one of said bits constituting said word.

6. The system of any one of preceding claims, wherein said information file includes the indication of the number of words to be transmitted.

7. The system of any one of the preceding claims, wherein said supervisor includes:

— reception means connected to said bus to receive signals transmitted by said interfaces; and

— transmission means capable of being connected to said bus to send instructions to said interfaces;

said means for storing the instructions being connected to said transmission means and said reception means and including a memory for storing and supplying said instructions, a logic circuit for selecting said instructions in said memory and a program counter incremented whenever an instruction is supplied to said transmission means.

8. The system of claim 7, wherein said supervisor further includes means for storing the number of words to be transmitted by information file, said number being included in one of the words of said information file supplied by the emitting source which has emitted the file, said means furnishing an end-of-file signal to said logic circuit when said number of words has been transmitted.

9. The system of any one of the preceding claims, further comprising a strategy logic circuit to determine an order of priority for connecting to said bus each of said interfaces having data to be transmitted at the same time, said strategy circuit comprising means for sequentially storing the requests from said interfaces which are in a condition to transmit at said instant, means for assigning an order of priority to said interfaces, and means for not taking into account any new data transmission request, at another moment, as long as said interfaces whose requests have been stored have not transmitted their data.

10. The system of claim 9, wherein said means for storing said requests from said interfaces which are in a condition to transmit include an assembly of J—K flip-flops, each corresponding to one of said interfaces and receiving on one of its two inputs a signal characteristic of the presence or of the

1595449 COMPLETE SPECIFICATION
18 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 1

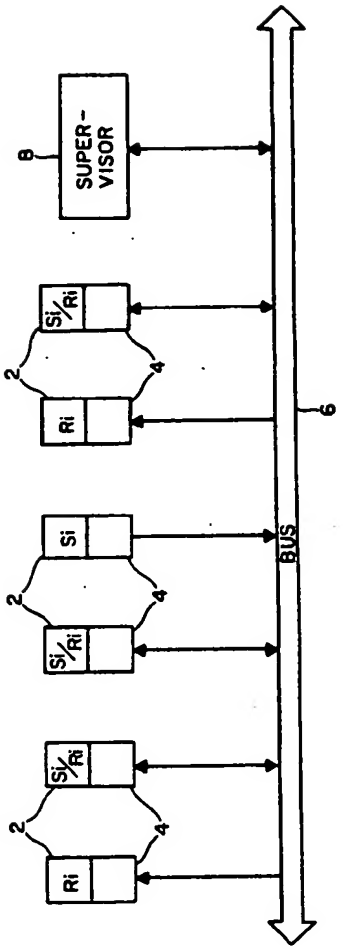

Fig. 1

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Sheet 3

Fig. 3

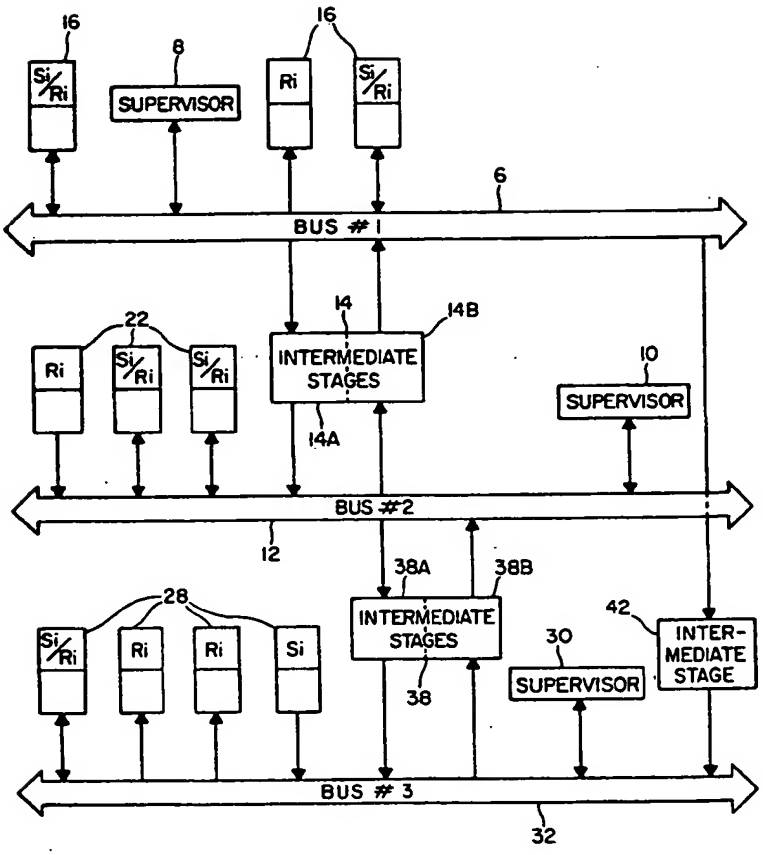
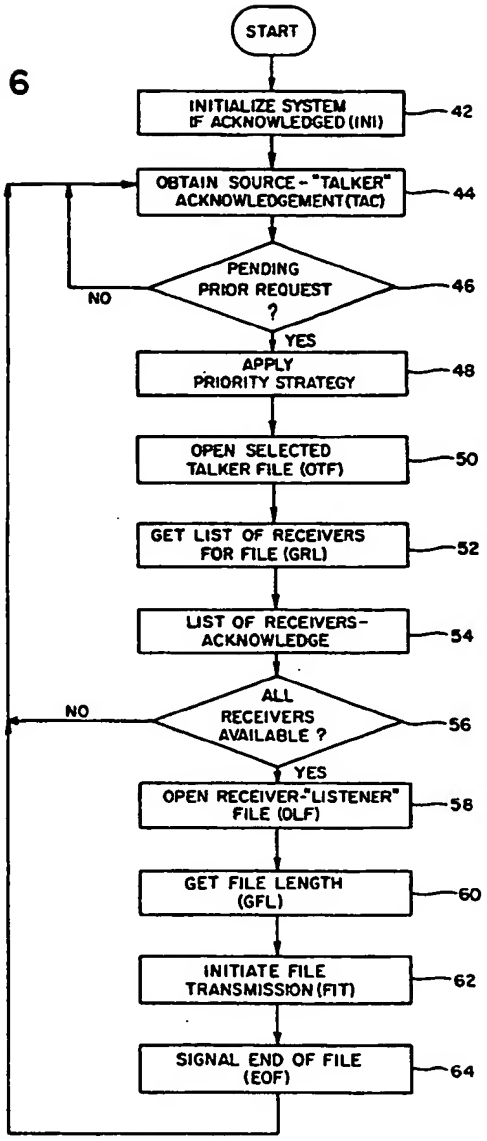


Fig. 6



1595449 COMPLETE SPECIFICATION
18 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheet 7

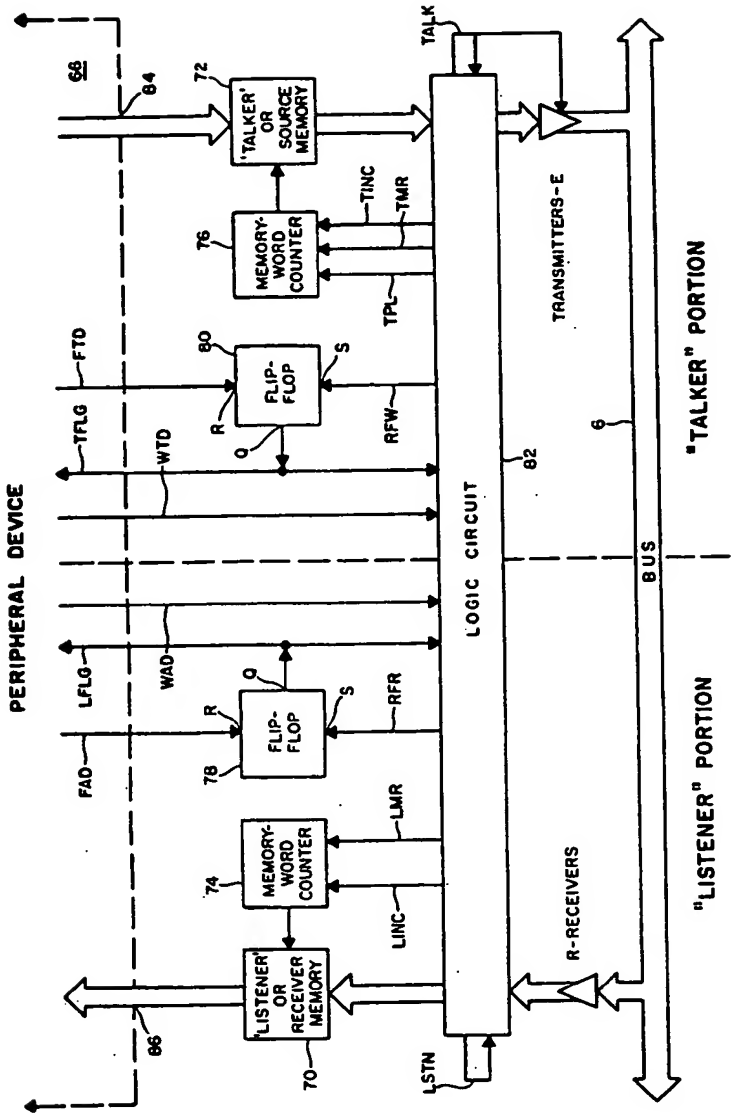


Fig. 8

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Sheet 9

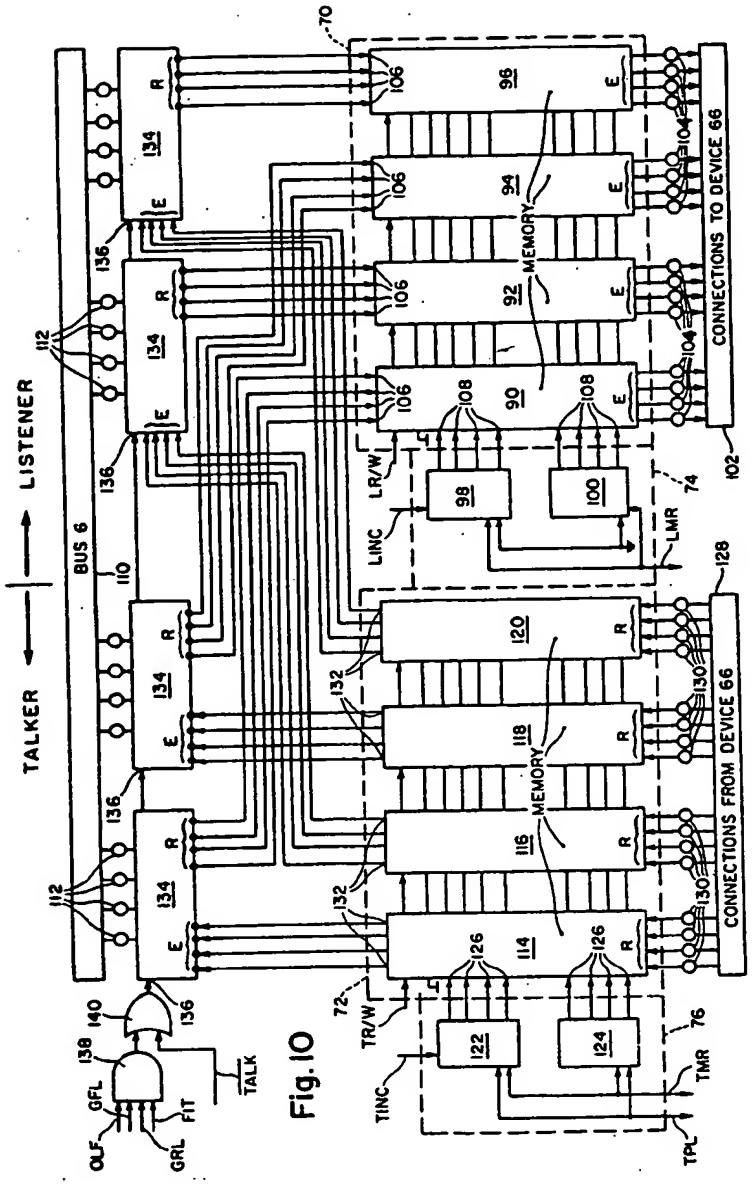


Fig. 10

Fig. 11B

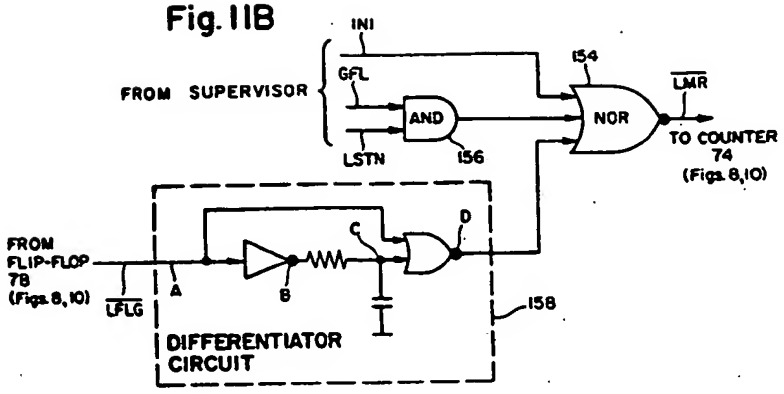


Fig. 11C

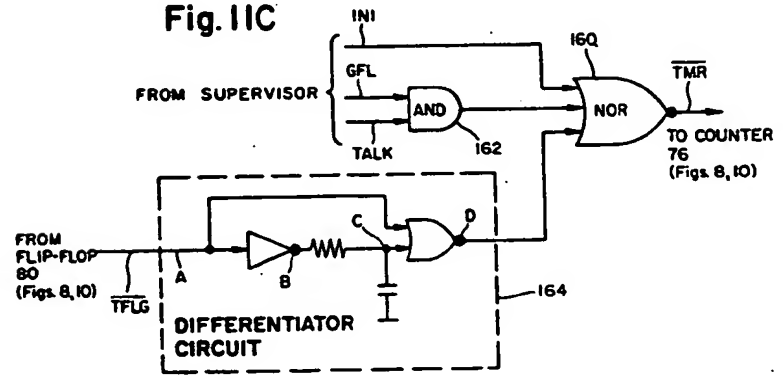
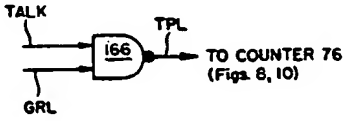


Fig. 11D



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Sheet 13

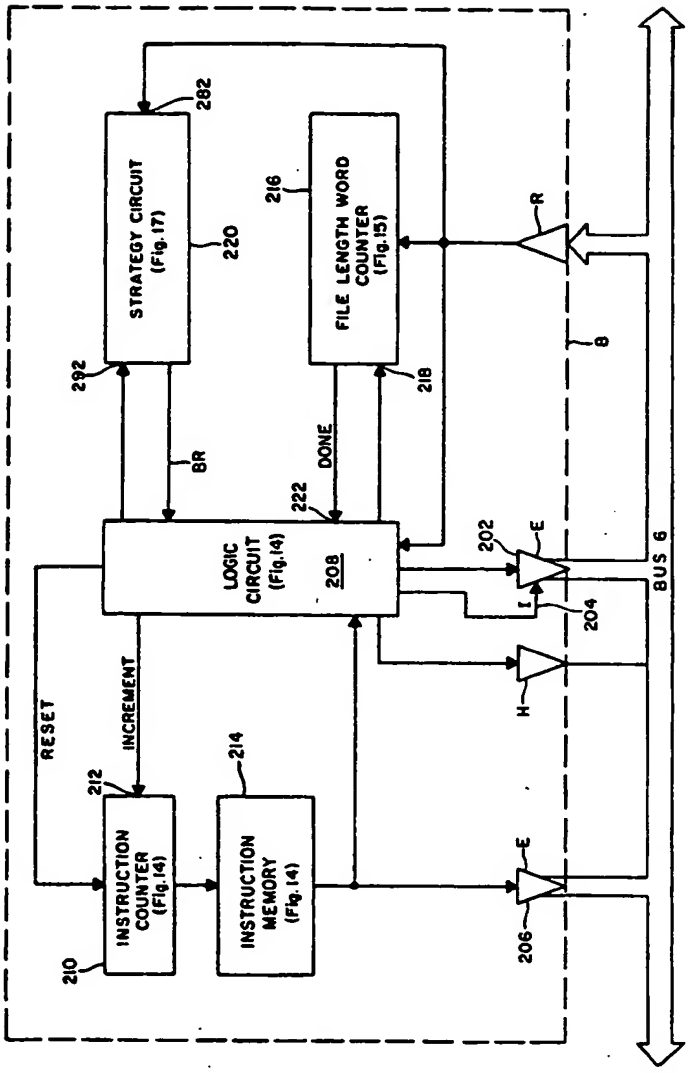

Fig. 13

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Sheet 15

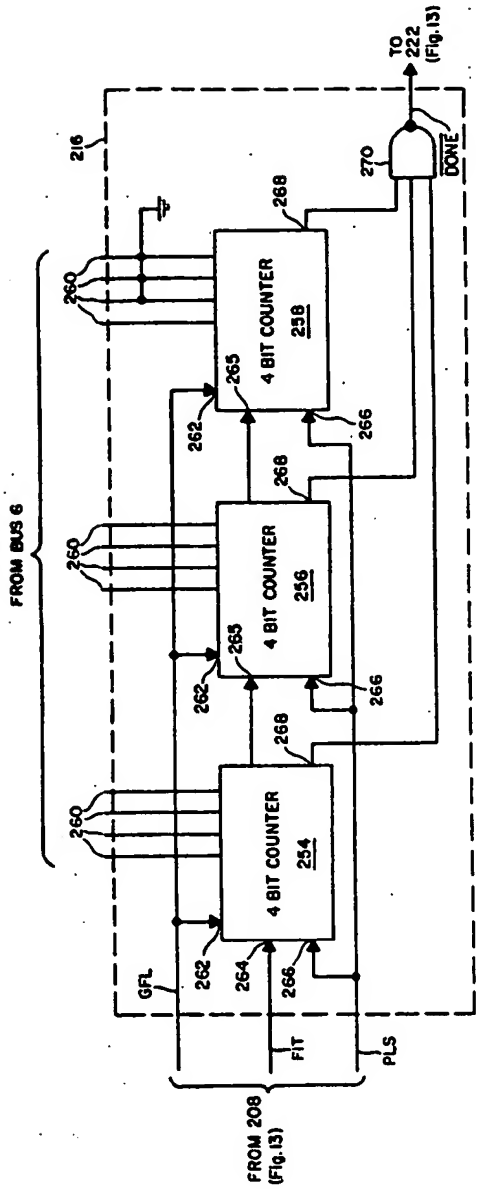
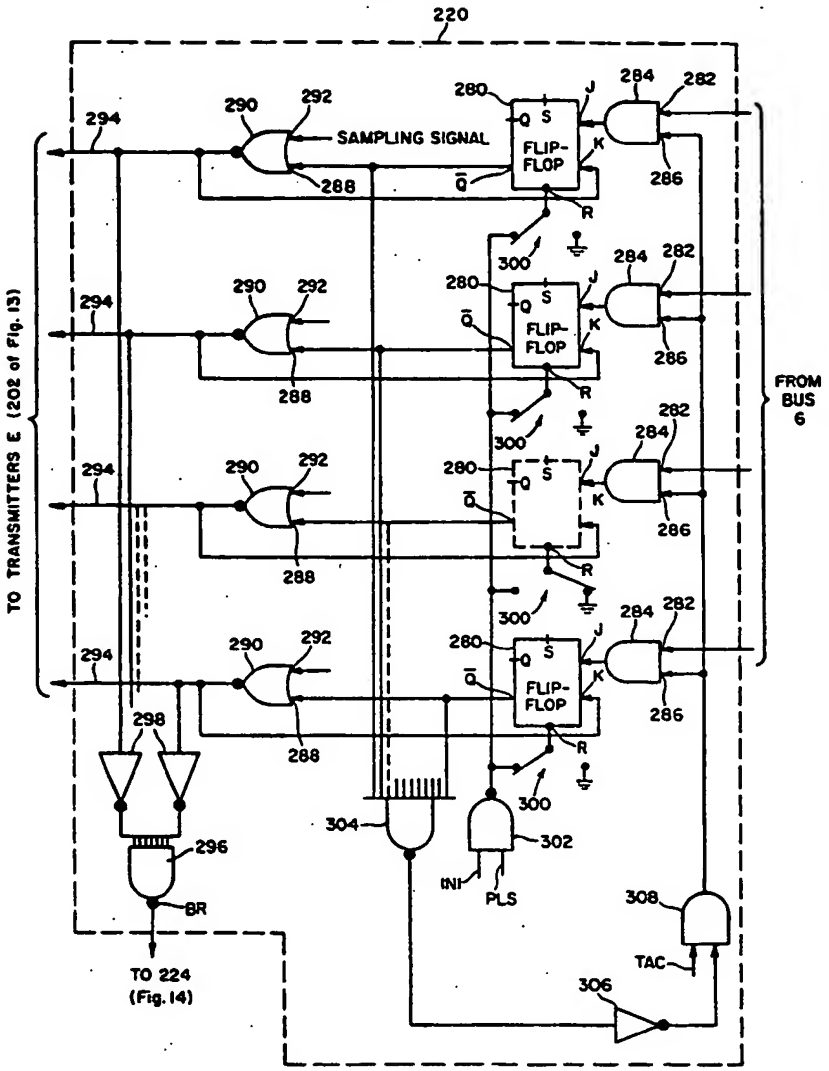


Fig.15

Fig. 17


220
TO TRANSMITTERS E (202 of Fig. 13)
FROM BUS 6
SAMPLING SIGNAL
FLIP-FLOP
TO 224 (Fig. 14)
INI
PLS
TAC
BR